CLAIMS

What is claimed is:

1. A method for determining and reducing an electrically charged state of a semiconductor process wafer comprising the steps of:

providing a metal filled via array in at least one level of multi-level device comprising a semiconductor process wafer the metal filled via array in electrical communication with at least one underlying metallization layer the metal filled via array further including a plurality of interspersed electrically isolated dummy metal portions to form a via array monitor;

exposing the semiconductor process wafer including the via array monitor to an electrical charge altering process including to produce an electrically charged state over at least a portion of the semiconductor wafer;

carrying out electrical measurements of the via array monitor to determine a level of the electrically charged state; and,

carrying out an electrically charge neutralizing process to reduce a level of the electrically charged state to a predetermined acceptable level prior to carrying out a subsequent process.

2. The method of claim 1, wherein the via array monitor is formed with a predetermined density of metal filled vias and electrically isolated dummy metal portions.

3. The method of claim 2, wherein the metal filled vias are formed in a rectangular shaped array comprising rows and columns of the metal filled vias.

4. The method of claim 3, wherein the dummy metal portions are interspersed periodically between one of the rows and the columns about equidistant from adjacent metal filled vias.

5. The method of claim 1, wherein the electrical charge altering process is selected from the group consisting of plasma-enhanced processes, chemical mechanical processes, and ultra-violet light exposure.

6. The method of claim 1, wherein the electrical charge altering process is selected from the group consisting of a reactive ion etch (RIE) process, an ashing process, a plasma treatment process, and an electrostatic dechucking process.

7. The method of claim 1, wherein the metal for forming the metal filled vias and the electrically isolated dummy metal portions is selected from the group consisting of copper, aluminum, tungsten, and alloys thereof.

8. The method of claim 1, wherein the via array monitor is provided within a plurality of wafer die comprising the semiconductor process wafer.

9. The method of claim 1, wherein the via array monitor is at least partially exposed in a level immediately underlying a metallization level following a plasma enhanced metal etching process.

10. The method of claim 9, wherein the level underlying a metallization level comprises tungsten plugs and the metallization level comprises AlCu metal interconnect lines.

11. The method of claim 10, wherein the subsequent process comprises a wet stripping process comprising hydroxyl ions.

12. The method of claim 1, wherein the charge neutralizing process comprises a plasma treatment with one of argon, helium, nitrogen, and hydrogen.

13. The method of claim 1, wherein the charge neutralizing process comprises applying one of a current and voltage to at least portions of the semiconductor process wafer.

14. The method of claim 1, wherein the steps of carrying out electrical measurements and carrying out an electrically charge neutralizing process are sequentially repeated to achieve the predetermined acceptable level.

15. The method of claim 1, wherein the step of carrying out electrical measurements is selected from the group of measurements consisting of resistance, impedance, and electrical charge.

16. A method for monitoring electrical properties in a micro-integrated circuit manufacturing process comprising the steps of:

providing a metal filled via array in at least one level of multi-level device comprising a semiconductor process wafer the metal filled via array of a predetermined density in electrical communication with at least one underlying metallization layer the metal filled via array further including a predetermined density of interspersed electrically isolated dummy metal portions to form a via array monitor;

exposing the semiconductor process wafer including the via array monitor to an electrical charge altering process including to produce an electrically charged state over at least a portion of the via array monitor; and,

carrying out electrical measurements of the via array monitor including at least one of resistance, impedance, and an

electrical charge to determine an electrical charge level prior to carrying out a subsequent process.

17. The method of claim 16, further comprising carrying out a charge neutralizing process and repeating the step of electrical measurements until the electrical charge level is within a predetermined acceptable range.

18. The method of claim 16, wherein the via array monitor is provided in each of the active die on a semiconductor wafer.

19. The method of claim 16, wherein the dummy metal portions are interspersed periodically about equidistant from metal filled vias forming the via array.

20. The method of claim 16, wherein the electrical charge altering process is selected from the group consisting of a reactive ion etch (RIE) process, an ashing process, a plasma treatment process, and an electrostatic dechucking process.

21. The method of claim 16, wherein the metal for forming the metal filled vias and the electrically isolated dummy metal portions is selected from the group consisting of copper, aluminum, tungsten, and alloys thereof.

22. The method of claim 16, wherein the via array monitor is at least partially exposed in a level immediately underlying a metallization level following a plasma enhanced metal etching process.

23. The method of claim 22, wherein the level underlying a metallization level comprises tungsten plugs and the metallization level comprises AlCu metal interconnect lines.

24. The method of claim 16, wherein the subsequent process comprises a wet stripping process comprising hydroxyl ions.

25. A via array monitor for measuring electrical properties of a semiconductor wafer portion comprising:

a metal filled via array in a dielectric insulating layer having an exposed surface comprising vias disposed in a die portion of a semiconductor process wafer;

the metal filled via array further comprising a predetermined via array size and via density each of the vias in electrical communication with at least one underlying metallization layer to allow an electrical property measurement of the vias;

the metal filled via array further comprising a predetermined density of electrically isolated dummy metal portions interspersed between the vias;

wherein the metal filled via array is configured to allow an electrical measurement including at least one of resistance, impedance, and electrical charge.

26. The via array monitor of claim 25, wherein the metal filled via array is rectangular shaped with a side measuring from about 1 to about 8 microns.

27. The via array monitor of claim 25, wherein the vias comprising the metal filled via array are formed into at least one of rows and columns.

28. The via array monitor of claim 27, wherein the electrically isolated dummy metal portions are interspersed periodically between the at least one of rows and columns.

29. The via array monitor of claim 28, wherein the electrically isolated dummy metal portions are interspersed about equidistantly from adjacent vias between the at least one of rows and columns from about every 3 to about every 8 of the at least one of rows and columns.

30. The via array monitor of claim 25, further comprising from about 5 to about 25 electrically isolated dummy metal portions per about 80 to about 100 vias.

31. The via array monitor of claim 25, wherein the electrically isolated dummy metal portions have about the same depth as the vias and are formed with a planar surface area larger than that of the vias by a factor of from about 1 to about 8.

32. The via array monitor of claim 25, wherein the metal filled via array comprises metal selected from the group consisting of copper, aluminum, tungsten, and alloys thereof.